THE INTERNATIONAL JOURNAL OF SCIENCE & TECHNOLEDGE

A Survey on Reconfigurable Architecture for 1-D DWT

Vimala M. S.
4th sem, M.Tech, VLSI & Embedded System, SSIT, Tumkur, India
Savitha C.
Assistant professor, Department of ECE, SSIT, Tumkur, Karnataka, India
Imran Rasheed
Assistant Professor, Department of ECE, MSRSAS, Bengaluru, Karnataka, India
Dr. M. Z. Kurian
HOD, Department of ECE, SSIT, Tumkur, India

Abstact:
A Reconfigurable architecture is mainly based on convolution method and in this paper it is done by utilizing lifting method. In lifting method, it reduces considerable hardware, computational complexity and also increases the speed where hardware resources are major components of DWT. Thus, by reducing hardware in turn increases speed. The architecture is classified into two modes for different throughput and bandwidth.

Key words: *DWT; Pipeline architecture*

1. Introduction

Wavelet transform is introduced by mallat where decomposition of samples into basic functions called wavelets on the orthogonal basis[1]. Thus, DWT does not contain any redundant data after transformation. Therefore, it leads to high compression ratio. If PSNR >40dB then the reconstructed samples are almost equivalent to original samples.

The DWT computation is based on two methods i.e. convolution and lifting methods. In convolution method has better scalability and regularity. If Ta and Tm are the delays of the adder and multiplier, respectively, then the critical path of the lifting based architecture for the (9, 7) filter is (4×Tm + 8×Ta), while that of the convolution implementation is (Tm + 2×Ta). The advantages of lifting method are, 1. Lifting leads to a speed-up when compared to the standard implementation. 2. Lifting allows for an in-place implementation of the fast wavelet transform, a feature similar to the Fast Fourier Transform. This means the wavelet transform can be calculated without allocating auxiliary memory. 3. All operations within one lifting step can be done entirely parallel while the only sequential part is the order of the lifting operations. 4. Using lifting it is particularly easy to build non linear wavelet transforms. Typical examples are wavelet transforms that map integers to integers. Such transforms are important for hardware implementation and for lossless image coding. 5. Using lifting and integer-to-integer transforms, it is possible to combine bi-orthogonal wavelets with scalar quantization and still keep cubic quantization cells which are optimal like in the orthogonal case.

In the present era, efficient design of DWT using 9/7 filters in resource constrained hand-held devices with capability for real-time processing of the computation intensive multi-media application is a necessary challenge. Multiplier-less hardware design provides a kind of solution to this problem due to its scope for lower hardware complexity and higher throughput of computation in lifting based pipeline architecture.

2. Literature Survey

The main feature of the lifting-based discrete wavelet transform scheme is to break up the high-pass and low-pass wavelet filters into a sequence of smaller filters that in turn can be converted into a sequence of upper and lower triangular matrices [4]. The basic idea behind the lifting scheme is to use data correlation to remove the redundancy. The lifting algorithm can be computed in three main phases, namely: the split phase, the predict phase and the update phase, as illustrated in Fig.1.

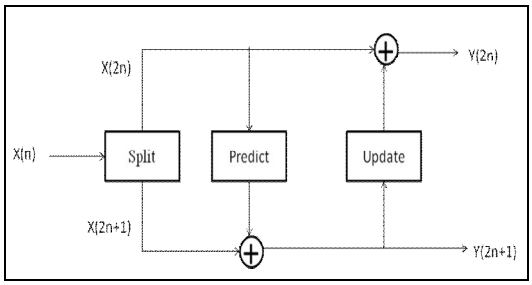

Figure 1: Split, predict and update phases of the lifting based DWT

Split phase, In this split phase, the data set x(n) is split into two subsets to separate the even samples from the odd ones:
Xe=X(2n), Xo=X(2n+1) (1)
Prediction phase, In the prediction stage, the main step is to eliminate redundancy left and give a more compact data representation. At this point, we will use the even subset x(2n) to predict the odd subset x(2n+1) using a prediction function P. The difference between the predicted value of the subset and the original value is processed and replaces this latter:
Y(2n+1) = Xo(2n+1) – P(Xe) (2)
Update phase. The third stage of the lifting scheme introduces the update phase. In this stage the coefficient x(2n) is lifted with the help of the neighboring wavelet coefficients. This phase is referred as the primal lifting phase or update phase:
Y(2n) = Y(2n+1) + U(Xe) (3)
Where, U is the new update operator.

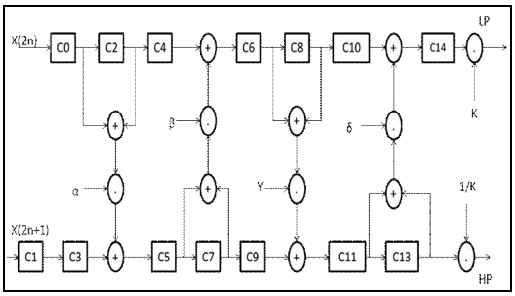

Figure 2: Pipelined architecture for 1-D DWT

The 1-D DWT architecture can be designed as a pipelined structure following the lifting scheme with 6 multiplier, 8 adders and 14 registers is as shown in fig.2. The bit length of DWT internal registers depends on their relative position inside the DWT pipeline. The registers located before alpha multiplication in the odd dataflow and before beta multiplication in the even dataflow store integers from -127 to 128(signed 8-bits). The registers located after beta multiplication in the odd dataflow and before gamma multiplication in the even dataflow store integers from -184 to 184(signed 9-bits). The registers located after gamma multiplication in the odd dataflow and before delta multiplication in the even dataflow store integers from -205 to 205(signed 9-bits). The registers located after delta multiplication in the odd dataflow and before division by k store integers from -366 to 366(signed 8-bits). The register located at output data of the even dataflow corresponds to low frequency of input image samples store values from -298 to 298(signed 10-bits). The register located at output data of the odd dataflow corresponds to high frequency of input image samples store values from -252 to 252(signed 9-bits). These 9 bits, even though a low magnitude value is expected for this data output due to the nature of the transform of still tone images[4].

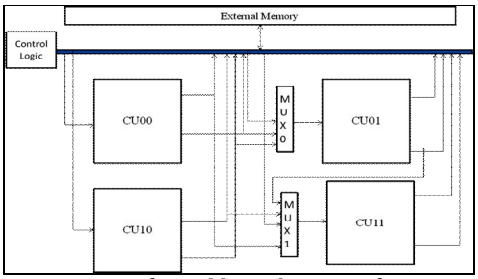

Figure 3: Reconfigurable architecture for MODE 1

In MODE1(cooperation among multiple CUs), all four CUs of reconfigurable block work on same decomposition level in parallel is as shown in Fig.3, Where high throughput is the major concern of the task and the bandwidth of the EX MEM is sufficient[3].

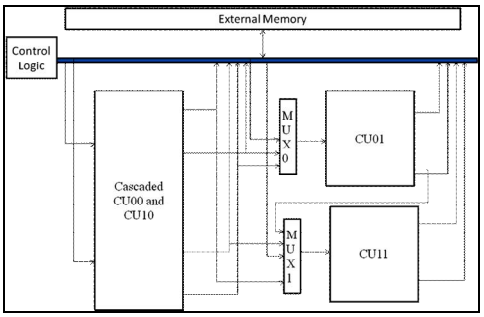

Figure 4: Reconfigurable architecture for MODE 2

In MODE 2(multi-level 1-D DWT), the circuit is considered as 3-level structure is as shown in Fig.4. The first level is composed of 2 CUs, which are CU00 and CU10, the second and the third level are separately built by CU01 and CU11. Since the number of operations of the second level is only half of the first level, the hardware resource required by the second level is also half of the first level. The efficiency of the CU11 is reduced to half by cascading CUs[3].

2.1. Recursive Pyramid Algorithm

The DWT can be looked at as the multi-resolution decomposition of a sequence[1]. It takes a length ***N*** sequence x(n) as input and generates a length ***N*** sequence as the output. The output has N/2 values at the highest resolution and N/4 values at the next resolution and so on i.e. the frequency resolution is low at the high frequencies and high at the low frequencies, whereas the time resolution is high at the higher frequencies and low at the lower frequencies. Let $X = 2J$, and let the number of frequencies or resolutions be J, i.e., considering J=logN octaves. Therefore, the frequency index j varies as 1,2,.., J corresponding to the scales $2^1, 2^2, \ldots, 2^J$.

The goals the RPA is set out to satisfy are as follows:

- Real-time performance (running DWT)
- Acceptance of input at a uniform, practical rate
- Minimization of storage (keep storage independent of input/ output size)
- Keeping the operation count comparable to the PA.

Total number of "computation" steps is 2 x (number of first octave outputs) = 2 x (N/2) = N and L multiplications and (L–1) additions, which is suitable for special purpose architecture and DSP chips.

The following are the main advantages of this algorithm:

- Since each output of the jth octave is scheduled at the "earliest" instance, only the latest L outputs of the (j - 1)st octave need to be stored. Thus, a total of at most L(log:Y - 1) words of storage is required. Note that it is L(log 3-1) and not L log X since the last octave output need not be stored.
- Due to its structure, it is highly amenable to systolic and pipelined approaches.
- It produces the output in an order that is ideal for many applications like sub-band coding and trans-multiplexers.
- The main disadvantage of the RPA is
- In general-purpose computers, the effort required to keep track of the latest L log N-L block of outputs might outweigh the reduction in storage requirements[2].

3. Application

- It is used in speech compression, which reduces transmission time in mobile applications
- It is used for real time audio and video compression.
- It is used in signal processing applications.
- It is mainly used for image compression.

4. Conclusion

In this paper, the reconfigurable architecture for 1-D DWT is reconfigured into two modes i.e. MODE1 and MODE2. The MODE of operation depends on control logic. The Approximation technique is used in pipeline architecture to increase the speed and to reduce the hardware.

5. References

1. S. G. Mallat, "A theory for multi-resolution signal decomposition: the wavelet representation," Pattern Analysis and Machine Intelligence, IEEE Transactions on, vol.11, pp.674-693,1989, doi: 10.1109/34.192463
2. M. Vishwanath, "The recursive pyramid algorithm for the discrete wavelet transform," Signal Processing, IEEE Transactions on, vol.42,pp.673-676,1994,doi10.1109/78.277863
3. Qing Sun, Jiang Jiang, Yongxin Zhu, Yuzhuo Fu., "A Reconfigurable Architecture for 1-D and 2-D DWT," Field Programmable custom computing machines, 21st Annual International IEEE Symposium on 978-0-7695-9/13, doi: 10.1109/FCCM.2013.23